Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

M.E DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Third Semester

Applied Electronics

VL4072 – CAD for VLSI Design

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	List out some of the VLSI design automation tools.	RE	1	2
2.	Define the term VLSI and list its primary design methodologies.	RE	1	2
3.	Differentiate strongly connected and weakly connected graphs.	UN	2	2
4.	What is computational complexity, and why is it significant in algorithm analysis?	UN	2	2
5.	Summarize the differences between partitioning and placement in the design process.	UN	3	2
6.	Explain the purpose of layout compaction in VLSI design.	UN	3	2
7.	Compare global and detailed routing in an integrated circuit.	UN	4	2
8.	What are the main objectives in routing during VLSI layout design?	RE	4	2
9.	Summarize the role of verification in the context of digital design and why it is crucial?	UN	5	2
10.	Differentiate simulation and logic synthesis.	UN	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	With a flowchart, analyze the different process involved in the physical design cycle of VLSI circuits.	AN	1	13
		Or			
	b	Compare full custom design and standard cell design styles. What are the pros and cons of each?	AN	1	13
12.	a	Compare depth first search and breadth first search algorithms used in graph theory for optimization of logic circuits.	AN	2	13
		Or			
	b	Compare and contrast tractable and intractable problems with relevant examples.	AN	2	13
13.	a	With the help of pseudo code, apply the Liao-Wong and Bellman-Ford algorithm for layout compaction.	AP	3	13
		Or			
	b	Apply partitioning techniques to a simple VLSI design problem and show the resulting partitions.	AP	3	13

14.	a	With a neat diagram, describe the shape functions and floor plan sizing of VLSI chips.	UN	4	13
		Or			
	b	Discuss the role of problem formulation in both floor planning and routing, and how it impacts the final layout.	UN	4	13
15.	a	Discuss how binary decision diagrams help in logic optimization and verification.	UN	5	13
		Or			
	b	Explain the event driven simulation method used to simulate the logic circuit at gate level.	UN	5	13

*PART – C (Marks 1*15 = 15)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
16.	a	Compare different placement algorithms, such as simulated annealing and min-cut algorithms, based on their effectiveness in optimizing area and performance.	AN	3	15
		Or			
	b	Analyze how left edge algorithm is used to solve channel routing problem. What specific characteristics of the algorithm make it suitable for this task.	AN	4	15